REMARKS

The claims remaining in the present application are Claims 1-36. Claim 11 has been amended. Claims 19-37 have been added. No new matter has been added as a result of these amendments.

CLAIM REJECTIONS

35 U.S.C. §103

CLAIMS 1-3

Claims 1-3 are rejected under 35 U.S.C. §102(e) as being unpatentable over Orton et al., U.S. Patent No. 6,118,306 (hereinafter, Orton) in view of "AX64PRO OR AK72?," Newsreader, June 15, 2000 (hereinafter, Newsreader). The rejection is respectfully traversed for the following reasons.

Independent Claim 1 recites, in part:

> reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled, wherein said value of the core voltage is not sufficient to maintain processing activity in said processor.

The cited combination does not teach or suggest these limitations. Orton may teach a mode in which the processor is not clocked, but Orton is nevertheless silent as to whether or not, in this mode, the processor would be capable of processing activity based on this mode's processor

voltage. Newsreader may disclose a deep-sleep function for a system having an AMD processor but is totally silent as to whether or not the processor is clocked in deep-sleep. In fact, relevant AMD specifications are clear that the processor used by Newsreader is clocked in all power management modes thereby implying that the Newsreader processor is clocked in deep-sleep. Regardless of whether or not the processor in Newsreader is clocked, like Orton, Newsreader is totally silent as to the processor's capability to perform processing activity while in the voltage level of its deep-sleep. Therefore, Newsreader, like Orton, does not teach or suggest the above claim limitations. These arguments are presented more fully below.

The rejection concedes that Orton fails to explicitly teach a method for reducing power used by a processor where the core voltage is set to a value that is not sufficient to maintain processing activity in said processor (when at a reduced voltage that is sufficient to maintain state). Applicants agree and respectfully assert that Orton fails to suggest these limitations.

Applicants respectfully assert that Newsreader fails to remedy these deficiencies in Orton in that Newsreader fails to teach or suggest the claim limitations missing in Orton. The rejection asserts that what is missing from Orton's teaching is reducing the processor core voltage to one Volt or less during deep sleep mode. Applicants respectfully disagree. Applicants

respectfully assert that, at a minimum, what is missing from Orton's teaching, among other things, is the claim limitation of "wherein said value of the core voltage is not sufficient to maintain processing activity in said processor."

Newsreader may disclose reducing core voltage to one Volt during a "deep sleep" function of a KineitiZ 7T mainboard, which Newsreader asserts is used with AMD Socket A Athlon™ processors. However, the deep sleep function is not described in any detail within Newsreader. Newsreader is silent as to the clocking of the processor during the deep sleep function. However, AMD's own specifications of the relevant time period specify that AMD processors are to be clocked while in all power management modes (see below). This implies that the Newsreader article discloses processor clocking during the deep sleep function. Moreover, regardless of the processor clocking state, Newsreader nevertheless does not disclose whether the processor is *capable* of executing instructions or not when held at the deep-sleep voltage level. Therefore, Newsreader does not teach the claim limitations of the core voltage being not sufficient to maintain processing activity in the processor.

For the foregoing reasons, the cited combination does not teach or suggest the claim limitations of reducing core voltage to a value sufficient to maintain state but not sufficient to maintain processing activity.

Next, Applicants respectfully assert the art does not suggest combining Orton and Newsreader in such a fashion to arrive at the claimed invention. Newsreader asserts that the KineitiZ 7T mainboard has a "deep-sleep" function in which the voltage to the processor is 1.0 Volt. Newsreader asserts that the KineitiZ 7T mainboard is used with AMD Socket A Athlon™ processors. It is Applicants understanding, which is based on AMD specifications, that AMD Athlon™ processors at approximately that time (both Socket A and Slot A) were required to clock to the processor in all power management states, as discussed above (see e.g., page 14 of AMD Athlon™ processor module datasheet, Publication # 21016, Revision M, June 2000 (Slot A); and page 14 of AMD Athlon™ processor model 4 datasheet, Publication # 23792 Revision K, November 2001 (Socket A)).

However, Claim 1 recites that the system clock is disabled when the value of the core voltage is not sufficient to maintain processing activity in said processor. Thus, the art does not suggest combining Newsreader's teaching of reducing processor voltage to 1.0 Volt (while clocking the processor because an AMD processor is required) with Orton's teaching of disabling the clock. Therefore, the art does not suggest combining Orton and Newsreader in such a fashion to arrive at the claimed invention. In fact, the cited art teaches away from the claimed combination.

Moreover, even if it is assumed that Orton's teaching is modified to drop the core voltage to Newsreader's 1.0 Volt, Applicants respectfully assert that the rejection has not established what would be the effect on the processor. For example, the rejection has not established what would be the effect of reducing the voltage to the processor in Orton (e.g., processor 12 in Figs. 1, 2, and 5) to any particular voltage during sleep mode. Applicants assert that it is understood that different processors have different operational characteristics. Therefore, Applicants do not understand the evidence in the record to establish that operating Orton's processor (12) at 1.0 Volt as being "not sufficient to maintain processing activity," as claimed.

For the foregoing reasons, the art does not suggest combining Orton and Newsreader in such a fashion to arrive at the claimed invention.

For all of the foregoing reasons, Claim 1 is neither taught nor suggested by Orton and Newsreader, alone or in combination. Therefore, Applicants respectfully request allowance of Claim 1.

Claims 2-3 depend from Claim 1, which is believed to be allowable for the foregoing reasons. As a result of their dependency, Claims 2-3 are believed to be allowable. Applicants earnestly request their allowance.

CLAIMS 4, 12 and 14-18

Claims 4, 12 and 14-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Orton and Applicant Admitted Prior Art (AAPA). The rejection is respectfully traversed for the following reasons.

CLAIM 4

Independent Claim 4 recites, in part:

> providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage (emphasis added).

Independent Claim 4 recites that a feedback signal is provided to the voltage regulator to reduce its output voltage below a specified output voltage. Applicants respectfully assert that neither Orton nor AAPA teach or suggest these claim limitations, alone or in combination.

The rejection concedes that Orton does not explicitly teach providing feedback to the voltage regulator. Applicants respectfully assert that Orton does not teach or suggest these limitations.

AAPA ("Maxim" specification, page 10) may teach how to raise the output voltage of the voltage regulator, but not to lower the output voltage, as claimed. Therefore, AAPA fails to teach or suggest the claim limitations.

For the foregoing reasons, Applicants assert that Independent Claim 4 is neither taught nor suggested by the combination of Orton and AAPA. Consequently, Applicants earnestly request that Claim 4 be allowed.

CLAIM 12

Independent Claim 12 recites, in part:

> means for reducing the selectable voltage below a level provided by the voltage regulator comprising:
>
> a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and
>
> the voltage regulator feedback circuit receiving a value from the voltage divider network (emphasis added).

Claim 12 recites that a voltage divider network is joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage. The rejection concedes that Orton does not teach the voltage divider network. Therefore, Orton does not teach or suggest "a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage," as claimed.

Applicants respectfully assert that AAPA does not teach the claimed "voltage divider network joined between the output terminal and a voltage source furnishing a value *higher* than the selectable voltage."

For the foregoing reasons, Applicants assert that Independent Claim 12 is neither taught nor suggested by the combination of Orton and AAPA. Consequently, Applicants earnestly request that Claim 12 be allowed.

CLAIMS 14-18

Independent Claim 14 recites, in part:

> a voltage source furnishing a value higher than the selectable voltage; and
>
> a feedback circuit coupled to the voltage source, the output terminal, and the voltage regulator feedback circuit.

For reasons discussed in the response to Claim 12, Applicants assert that Independent Claim 14 is neither taught nor suggested by the combination of Orton and AAPA. Consequently, Applicants earnestly request that Claim 14 be allowed.

Claims 15-18 depend from Claims 4 and 14. By virtue of their dependency from a claim that is believed to be allowable, Applicants believe Claims 15-18 to be allowable.

35 U.S.C. §102

Claims 5-11 and 13 are rejected under 35 U.S.C. §102(a) or (e) as being anticipated by Orton. The rejection is respectfully traversed for the following reasons.

CLAIMS 5 and 6

Independent Claim 5 recites, in part:

> transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled (emphasis added).

The underscored language refers to modes of operating the voltage regulator (power dissipation mode/power saving mode). The Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 5. Orton may discuss reducing power consumption (see, e.g., col. 2, lines 18-20). Orton may achieve a reduction in power by, for example, reducing the operating frequency of the processor. However, power savings can be achieved in manners other than reducing frequency and/or reducing voltage. Applicants have specifically recited in this embodiment that saving power is performed by a choice of mode of operation of the voltage regulator. Orton is silent as to operating the voltage regulator in a mode in which power is dissipated to a mode in which power is saved, as claimed. Thus,

Orton fails to teach or suggest the claimed transferring the operation of a voltage regulator from a mode in which power is dissipated to a mode in which power is saved, during a voltage transition.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 5. Therefore, Applicants earnestly request allowance of Claim 5.

Claim 6 depends from Claim 5. By virtue of its dependency on a claim that is believed to be allowable, Applicants believe Claim 6 to be allowable.

CLAIMS 7-10

Independent Claim 7 recites, in part:

> means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode, wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor (emphasis added).

For at least the reasons discussed in the response to Claim 1, Claim 7 is neither taught nor suggested by Orton. As such, Applicants earnestly request allowance of Claim 7.

Claims 8-10 depend from Claim 7. By virtue of their dependency from a claim that is believed to be allowable, Applicants believe Claims 8-10 to be allowable.

CLAIM 11

Currently Amended Independent Claim 11 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output (emphasis added).

Orton may describe causing the voltage regulator to output different voltages. However, Applicants respectfully assert that Orton is silent as to causing the voltage regulator to output a voltage below a lowest level the voltage regulator is specified to output, as claimed. Applicants respectfully assert that one of ordinary skill in the art would understand Orton to teach that the output voltage of the voltage regulator to be within a range specified by the voltage regulator, as Orton is silent as to causing the voltage regulator to output a voltage outside of that range.

For the foregoing reasons, Applicants respectfully assert that Orton fails to teach or suggest the limitations, "means for reducing the selectable

voltage below a lowest level the voltage regulator is specified to output."

Therefore, Applicants earnestly request allowance of Claim 11.

CLAIM 13

Claim 13 recites, in part:

> a voltage regulator having:
>
> an output terminal providing a selectable voltage, and
>
> an input terminal for receiving signals indicating the selectable voltage level;
>
> ...
>
> circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and
>
> means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases (emphasis added).

Applicants respectfully assert that Orton fails to teach or suggest the limitations of Claim 13. The rejection asserts that Orton teaches a battery (60) as a charge storage unit. However, while a battery may be capable of storing charge, Applicants respectfully assert that Orton does not teach or suggest how charge from the voltage regulator is stored in the battery, as claimed. Moreover, Applicants respectfully assert that Orton fails to teach or suggest how charge from the voltage regulator is stored in the battery when the selectable voltage decreases, as claimed.

For the foregoing reasons, Orton fails to teach or suggest the limitations of Claim 13. Therefore, Applicants earnestly request allowance of Claim 13.

NEW CLAIMS

Claims 19-37 have been added. No new matter has been added as a result of these claim amendments.

New Independent Claim 19 recites, in part:

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time

Applicants respectfully assert that the cited prior art fails to teach or suggest these limitations.

New Independent Claim 25 recites, in part:

> wherein a transition time for changing from said sleep voltage directly to said second operating voltage is greater than said allowed time for transitioning from said sleep state to said operating state.

Applicants respectfully assert that the cited prior art fails to teach or suggest these limitations.

New Independent Claim 29 recites, in part

> a first operating voltage that, based on a rate of transitioning from said sleep voltage to said first operating voltage, is not achievable from said sleep voltage within an allowed time for transitioning from a sleep state to an operating state.

Applicants respectfully assert that the cited prior art fails to teach or suggest these limitations.

New Independent Claim 33 recites, in part

> a first operating voltage when transitioning from said first sleep voltage; and
>
> a second operating voltage when transitioning from said second sleep voltage

Applicants respectfully assert that the cited prior art fails to teach or suggest these limitations.

Claims 20-24, 26-28, 30-32 and 34-37 depend from Claims 19, 25, 29, and 33, which are believed to be allowable for the foregoing reasons. Therefore, Claims 20-24, 26-28, 30-32 and 34-37 are believed to be allowable by virtue of this dependency.

CONCLUSION

In light of the above listed amendments and remarks, allowance of Claims 1-37 is requested.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: 3/22, 2005

Ronald M. Pomerenke
Registration No. 43,009

Address: WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113

Telephone: (408) 938-9060 Voice
(408) 938-9069 FAX